

**RESEARCH ON SPOKEN LANGUAGE PROCESSING**  
Progress Report No. 19 (1993-1994)  
*Indiana University*

**Implementation of a PC-Based Perceptual Testing System (PTS):  
A First Milestone<sup>1</sup>**

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<sup>1</sup>The development of this system was supported by NIH Research Grant DC00111 and NIH Training Grant DC-00012 to Indiana University, Bloomington.

## **Abstract**

This report describes the implementation of the first milestone in the development of a new PC-based perceptual testing system as proposed in Progress Report #18 (see Hernandez, Carrell, Reutter & Bernacki, 1992) along with some results of our functional test. We describe how we configured the system in order to meet our functional and operating requirements. We also describe the hardware components of the single station system, as well as some software implementation issues. To conclude, we will review our next milestone which will network the single station personal computers into an integrated system.

# **Implementation of a PC-Based Perceptual Testing System (PTS): A First Milestone**

## **Overview**

This project has several basic goals. The first was to design a replacement for the aging PDP-11/34-based real-time experiment control systems used in our laboratory since the early 1970's (see Forshee & Nusbaum, 1984). This was necessary because support for these mini-computer based systems has become virtually nonexistent both in terms of hardware and software. Furthermore, the architecture is 25 years old and, by modern standards, it is an extremely difficult environment in which to develop new robust applications. The second goal of the project was to develop an environment in which a variety of experimental tasks are possible that would be difficult or impossible to perform with existing equipment. The third goal of this project was to develop a system which is useful enough and inexpensive enough for researchers in speech perception and other related behavioral testing fields to implement in their own laboratories. Individual scientists' productivity may be greatly enhanced by the sharing of common tools. This will benefit both the developers of this project and the recipients of our development efforts.

As currently configured, the hardware and software combination can perform all of the basic experimental paradigms as well as the PDP-11 can. There are several important added benefits that were accomplished by this implementation, including high-resolution color visual displays, 16-bit 44.1 kHz audio output and 250 ns timing accuracy.

## **Implementation of Milestone 1 (Short-term Plans)**

The first milestone was to duplicate and improve the existing control facilities (see Hernandez, Carrell, Reutter & Bernacki, 1992) of the PDP-11/34 and LABLIB (Forshee, 1979) on a 386 PC-clone.

### **Hardware**

We have found the hardware combination described below to work very well together and to have passed all of our tests. We hope that this description will help other researchers in deciding the type of components needed in order to achieve the duplication of this system. See appendix A for a list of hardware specifications.

**CPU** - Even though we started our development on a PC-clone based on an Intel 386 chip, it was eventually replaced with a 486 PC-clone given the cost and the low demand for the older chip. We decided on a Mini-Tower case since it allowed for a higher wattage power supply, easy internal access, enough expansion slots for future development, and ease of placement on the work area.

The system has been successfully run with Phoenix 1.10 and Award Modular 4.50G BIOS. We have not tested the system on non-Intel based computers.

**Video Controller and Monitor** - We have used several different SVGA video controllers that have successfully worked. All of our video boards, however, have been Hercules compatible. We have been careful when selecting our monitors that it meets our requirement of .28 dot pitch and 1024x768 resolution.

**Timer** - In order to achieve the timing resolution needed for many of our experiments we used a high-resolution timing card from Alpha Logic Technologies called STAT. The ISA card uses a 32-bit timer with a resolution of 250 ns.

**Audio I/O** - We are currently using a Creative Labs SoundBlaster AWE32 sound board for digital sound output. This board provides 8-bit and 16-bit resolutions with programmable 5 kHz to 45 kHz sampling rates. It comes with a standard 512K RAM that can be upgraded to 28MB. We found this board to be very versatile and expandable. One upgrade option that we might need for later development is the Advance Signal Processing chip. Our tests show a total harmonic distortion (THD) of 0.05% with 1 kHz (0.94vrms and 2vrms @ 8 ohm loads). The output noise is approximately 0.33mvrms. This noise seems to be periodic and high frequency, perhaps due to the computer's internal clocks (reference to 4vrms output = -81.7 dB). The tests were done with an Hewlett Packard Model 334A Distortion Analyzer. We are using Beyerdynamic model DT-100 (400 Ohms) headphones for output to subjects.

**Response Boxes** - The response boxes were fabricated using three components. The first, a dedicated parallel port from Metrobyte model PIO-12 with 24 digital input/output lines. The second component is an interface to the PIO-12. It is responsible for triggering the occurrence of an event as fast as possible (approximately 100 ns). This piece of hardware was custom built by the Psychology Department's Electronic Shop. The last component, is the actual response box which was also built for us using non-tactile form-C (single pole double throw) buttons.

We decided to configure this part of the system in this manner after we failed to obtain consistent and accurate measures from the keyboard and keyboard port. We found that even though the error was consistent (about 16 to 20 msec, depending on the keyboard) on the keyboard input, the CPU high-resolution clock was not maintaining our 1-msec timing accuracy.

We realize that we have not met one of our requirements which was to use "off the shelf" components but we found this to be our only solution given what we had at the time. An "off the shelf" option to the digital I/O port might be Tucker Davis Special Parallel port. It has similar features but we have not addressed this option in our current configuration.

## Software

This section will not discuss every routine that was created for this first pass of programming but we describe those that have a special relationship with the hardware and those that form the core of the system. All routines are implemented using Microsoft C/C++ (only standard ANSI C is used) and some Assembly language under the DOS operating system. The routines are implemented in different modules in an effort to maintain the code as modular as possible.

Modifications to AUTOEXEC.BAT and CONFIG.SYS were needed to obtain the maximum amount of conventional memory. We also needed to be careful not to conflict with any of the base addresses, interrupts or DMA channels among the timer, audio, digital I/O and ethernet cards or with anything else in the system.

At this stage of development, all of the network activity is switched off when an experiment is running in order to maintain system integrity.

**CPU and Timers** - To achieve the type of attention needed to start and stop the timer board we had to implement an interrupt strategy. In our particular hardware configuration, we set the digital I/O board to trigger interrupt number three on our hardware. Whenever a button is pressed and this interrupt is triggered, an interrupt service routine (ISR) simply stops the timer; assuming that it had been started previously. The ISR disables all other interrupts while it is servicing itself, stops the clock, sets control back to the CPU, and allows other interrupts to occur. Two routines *BBallowresponse* and *BBignoreresponse* tell the CPU when and when not to pay attention to the button box events.

**Video** - Almost all of the video routines are implemented using Genus Graphics programming routines. In an effort to present visual data at a consistent rate, we developed a couple of routines that turn the video display ON and OFF (these routines are programmed at the video controller level). This strategy insures that the video raster will start at the left upper corner of the display. Since the image can be stored into memory before the video is actually turned ON, there will not be a time where the bottom half of the visual information will be displayed before the top portion (or where ever the raster happens to be when we ask it to display the video image). We realize that it will take approximately 15 ms for the raster to traverse down the screen (depending on the monitor refresh rate) but at least this error will be constant and the raster will be in the same starting position consistently.

**Audio I/O** - We used the Sound Blaster developers kit to implement all of our sound I/O routines. These are low-level enough meet our needs. Sound can be played both in the foreground or background via an interrupt and a dynamic memory access channel (DMA) set at the installation of the sound board. We intend to do more testing to establish what the gain values correspond to on a dB scale in order to implement programmable attenuators.

## **The Next Milestone (Milestone 2)**

During the next year, we will proceed to our next goal, which is networking the single station PTS system. The overall strategy will be to use one PC per testing station with each PC networked to a central "experiment server" PC. The central PC will coordinate the action of the testing station PCs on a block-by-block basis, if needed. It will also perform data and stimulus management and backup functions. The purpose of central control, as opposed to simply running a number of independent PC subject stations, is to make the experimenter's life easier. For example, facilities will be included to run multiple subjects in synchrony for simpler experiments. Also, we would like to know when subjects complete their task in order for us to automatically load a filler exercise to keep them from interrupting other subjects who have not completed the experiment.

**Phase 1.** Port experiment control system to a client/server model. Independent PCs should recognize that they are connected to a controller, and if they are, request services from that controller. If they are not, they should run the experiment locally in single-subject mode. In this phase, the subject station PCs should ask the server which experiment to run, which stimuli to use, where to put the data, and when to begin each block. Ideally communication will be via TCP/IP over 10-baseT Ethernet.

**Phase 2.** Develop block-by-block central data backup. Develop an experiment logbook database. Finalize network strategy.

**Phase 3.** Beta test experiment control system with network. Debug and revise system based on conducting several independent and block-to-block experiments.

## Summary

In summary, we have made substantial progress in developing and implementing a new PC-based perceptual testing system in our laboratory to replace the old PDP-11/34 system. The new system not only can perform all the functions of the old system, but it has a number of additional novel capabilities that will permit us to carry out a wide variety of behavioral experiments using speech and graphics output.

## References

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- Hernandez, L.R., Carrell, T.D., Reutter, J.G. & Bernacki, R.H. (1992). A new PC-based real-time experiment control system. *Research on Speech Perception Progress Report No. 18*, Bloomington, IN: Indiana University, pp. 243-253.

## Appendix A

### Current Hardware Specifications

A/D/A: Creative Labs Sound Blaster AWE16.

- Sample rate of 44.1 Khz, two channels with over sampling D/A
- On-board anti-alias filters
- Onboard buffer RAM of at least 256k bytes
- 16 bit resolution, > 80dB S/N
- ISA bus compatible

Response Boxes: IU Psychology Dept. Electronic Shop response box

#### General Description

- Quiet
- Good tactile feel
- Register response on down only
- Travel distance on the order of a few mm, with non-linear pressure (press hard and fall through to end).
- Spacing should be approx. 1 inch.
- No "smarts" in button box. Use just switches and lights. No need for "fancier" feedback like LCDs.

#### Feedback Lamp

- Mechanically robust
- Low power, high efficiency
- at least 100 mcd

#### Digital Input

- Latched level sensitive inputs
- Capable of maskable interrupt generation on bit change
- 8 bits or more

Timer: Alpha Logic Technologies STAT!

- resolution to 250 ns
- interrupt capability
- ease of programming

Video Monitor: Samsung Model SyncMaster 4Ne

- SVGA (1024x768)
- .28 dot pitch.
- Vertical refresh rate of 72 Hz or greater, non-interlaced.
- Horizontal, 55 Khz (18 microsecond refresh).

Network: 3Com Ethernetlink III

- thin wire or twisted pair Ethernet- 10-base-T